2.6 Instructions, Sorted by ISA

This section lists the instructions that are a part of the MIPS32 and MIPS64 ISAs.

2.6.1 List of MIPS32 Instructions

Table 2-1 lists of those instructions included in the MIPS32 ISA.

Table 2-1 MIPS32 Instructions

ABS.D	ABS.PS[1]	ABS.S	ADD	ADD.D	ADD.PS[1]	ADD.S	ADDI
ADDIU	ADDU	ALNV.PS[1]	AND	ANDI	BC1F	BC1FL	BC1T
BC1TL	BC2F	BC2FL	BC2T	BC2TL	BEQ	BEQL	BGEZ
BGEZAL	BGEZALL	BGEZL	BGTZ	BGTZL	BLEZ	BLEZL	BLTZ
BLTZAL	BLTZALL	BLTZL	BNE	BNEL	BREAK	C.cond.D	C.cond.PS[1]
C.cond.S	CACHE	CEIL.L.D[1]	CEIL.L.S[1]	CEIL.W.D	CEIL.W.S	CFC1	CFC2
CLO	CLZ	COP2	CTC1	CTC2	CVT.D.L[1]	CVT.D.S	CVT.D.W
CVT.L.D[1]	CVT.L.S[1]	CVT.PS.S[1]	CVT.S.D	CVT.S.L[1]	CVT.S.PL[1]	CVT.S.PU[1]	CVT.S.W
CVT.W.D	CVT.W.S	DERET	DI[2]	DIV	DIV.D	DIV.S	DIVU
EHB[2]	EI[2]	ERET	EXT[2]	FLOOR.L.D[1]	FLOOR.L.S[1]	FLOOR.W.D	FLOOR.W.S
INS[2]	J	JAL	JALR	JALR.HB[2]	JR	JR.HB[2]	LB
LBU	LDC1	LDC2	LDXC1[1]	LH	LHU	LL	LUI
LUXC1[1]	LW	LWC1	LWC2	LWL	LWR	LWXC1[1]	MADD
MADD.D[1]	MADD.PS[1]	MADD.S[1]	MADDU	MFC0	MFC1	MFC2	MFHC1[2]
MFHC2[2]	MFHI	MFLO	MOV.D	MOV.PS[1]	MOV.S	MOVF	MOVF.D
MOVF.PS[1]	MOVF.S	MOVN	MOVN.D	MOVN.PS[1]	MOVN.S	MOVT	MOVT.D
MOVT.PS[1]	MOVT.S	MOVZ	MOVZ.D	MOVZ.PS[1]	MOVZ.S	MSUB	MSUB.D[1]
MSUB.PS[1]	MSUB.S[1]	MSUBU	MTC0	MTC1	MTC2	MTHC1[2]	MTHC2[2]
MTHI	MTLO	MUL	MUL.D	MUL.PS[1]	MUL.S	MULT	MULTU
NEG.D	NEG.PS[1]	NEG.S	NMADD.D[1]	NMADD.PS[1]	NMADD.S[1]	NMSUB.D[1]	NMSUB.PS[1]
NMSUB.S[1]	NOR	OR	ORI	PLL.PS[1]	PLU.PS[1]	PREF	PREFX[1]
PUL.PS[1]	PUU.PS[1]	RDHWR[2]	RDPGPR[2]	RECIP.D[1]	RECIP.S[1]	ROTR[2]	ROTRV[2]
ROUND.L.D[1]	ROUND.L.S[1]	ROUND.W.D	ROUND.W.S	RSQRT.D[1]	RSQRT.S[1]	SB	SC
SDBBP	SDC1	SDC2	SDXC1[1]	SEB[2]	SEH[2]	SH	SLL
SLLV	SLT	SLTI	SLTIU	SLTU	SQRT.D	SQRT.S	SRA
SRAV	SRL	SRLV	SSNOP	SUB	SUB.D	SUB.PS[1]	SUB.S
SUBU	SUXC1[1]	SW	SWC1	SWC2	SWL	SWR	SWXC1[1]
SYNC	SYNCI[2]	SYSCALL	TEQ	TEQI	TGE	TGEI	TGEIU
TGEU	TLBP	TLBR	TLBWI	TLBWR	TLT	TLTI	TLTIU
TLTU	TNE	TNEI	TRUNC.L.D[1]	TRUNC.L.S[1]	TRUNC.W.D	TRUNC.W.S	WAIT
WRPGPR[2]	WSBH[2]	XOR	XORI				

1. In Release 1 of the Architecture, these instructions are legal only with a MIPS64 processor with 64-bit operations enabled (they are, in effect, actually MIPS64 instructions). In Release 2 of the Architecture, these instructions are legal with either a MIPS32 or MIPS64 processor which includes a 64-bit floating point unit.
2. These instructions are legal only in an implementation of Release 2 of the Architecture