Bachelor in Computer Science Engineering

Course information

Year 2021-22

GENERAL SPECIFICATIONS			
English name			
Computer Fundamentals			
Spanish name			
Fundamentos de Computadores			
Code	**Type**		
606010108	Fundamental		
Time distribution			
	Total	**In class**	**Out class**
Working hours	150	60	90

ECTS:				
Standard group	**Small groups**			
	Classroom	**Lab**	**Practices**	**Computer classroom**
4.14	0	1.86	0	0

Departments	**Knowledge areas**
Ingeniería Electrónica, Sistemas Informáticos y Automática	Ingeniería de Sistemas y Automática
Year	**Semester**
1st	1st

TEACHING STAFF			
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SPECIFIC INFORMATION OF THE COURSE
1. Contents description
1.1. In English:
Combinational systems. Sequential systems. Introduction to computer systems.
1.2. In Spanish
Sistemas combinacionales. Sistemas secuenciales. Introducción a los sistemas computadores.
2. Background
2.1.Situation within the Degree:
The course provides a structured view of the design of digital systems which are the key ingredient in the computer systems' building. This training is furthermore basic to face the study of other courses within the undergraduate degree such as: *Estructura de Computadores* and *Arquitectura de Computadores* from the second year. *Diseño de Sistemas Hardware-Software* and *Sistemas Programables* both from the third year

2.2. Recommendations:

No previous knowledge is required to face the study of this course, because this is a basic type course within the undergraduate degree.

Although, it is advisable that the student would have basic knowledge on IT-system resources and about its usage in Windows environments.

3. Objectives (as result of teaching):

To qualify the student for the digital system analysis and to feature its operation.

To qualify the student to design a digital system fully operating, from some non-formal initial specifications.

To make use, for the analysis and design of the course practices, of the provided tools: technical manuals, software for the edition, design and simulation; integrated electronic devices; logical trainers and basic-measure apparatus from the laboratory.

4. Skills to be acquired

4.1. Specific Skills:

CB3. Gather and interpret relevant data (usually within their area of study) to make judgments that include a reflection on relevant social, scientific or ethical issues.

CC09: Skill to know, understand and assess the structure and the architecture of the computers as well as the basic components which comprise them.

4.2. General Skills:

CG0: Analysis and synthesis skill: To find, analyze, criticize (critical reasoning), structure and synthetize information from diverse sources as well as combine ideas and knowledge.

G03: Solving problem skill.

G04: Skill to make decisions based on objective criteria (experimental, scientific or simulation-based data) as well as skill to argue and justify logically the aforementioned decision, being able to accept other point-of-views.

G05: Team-work skill.

TC2. Develop a critical attitude, being able to analyze and synthesize.

TC3. Develop an attitude of inquiry that permanently enables to review and deepen in the knowledge.

TC4. Acquire Computer and Information Skills (CI2) and apply them working.

5. Training Activities and Teaching Methods

5.1. Training Activities:

- Theory sessions on the program contents.
- Problem solving sessions.
- Practical sessions in specialized laboratories or in Computer Science rooms.
- Faculty-Guided academic activities (FGAA): seminars, keynotes, work developments, discussions, collective tutorials, assessment and self-assessment activities.

5.2. Teaching Methods:

- Participative lecture.
- Development of Practices in Specialized Laboratories or Computer Science Rooms in small groups.
- Problem solving and practical exercise.
- Individual or collective tutorials. Direct feedback faculty-students.
- Assessments and exams

5.3. Development and Justification:

Theoretical and problem lessons

In the 41.4 hours devoted to the theoretical sessions, lectures for the whole group will be lectured, where the course theoretical-base will be explained and will be expounded clarifying problems from the same. Two weekly sessions will be lectured with a duration for both, equally of one hour and thirty minutes and one hour and fifteen minutes and will be alternated with the problem sessions throughout the academic period (four-month period) in such a way that once a didactical unit is finished with its corresponding academic theoretical sessions, the problem sessions will be done. The methodology for lecturing the theory and the clarifying samples will be the introduction by means of the blackboard and the projection of slides (which will be made in a IT-system tool). The lecturer may ask for the active participation of the student by means of fast questions, taking into account the students who intervene more for the assessment moment.
In the webpage of the course, the presentations and other reference needed materials for the session follow-up will be found. It is very important that the student complete the information from the slide with his/her own class notes, because the provided slides are not the lecture notes of the course.

Laboratory practices

The 18.6 hours of practices' sessions will take place in the laboratory, making use of computers with simulation software and practice trainers, as well as development cards for the circuit implementation. In every practice session, the analysis and/or design and implement of a digital system will be conducted, which may help to assimilate the concepts studied in the theoretical sessions. Via the course webpage, the wordings of the different practices to carry out and the additional material to solver will be provided; in this way, the students will have the problem to be solved ahead of time as well as the work methodology. Before attending the session, the students must have made the solving of the corresponding practice with the goal of getting the results which will be confirmed later in the laboratory. 13 laboratory sessions will be lectured and 8 practices will be done. The first practice will be introductory and will cover the lecturing of the set of instruments from the laboratory as well as the simulation software to be used in the first four practices. The remaining 7 practices will consist of exercises on analysis and/or design of digital systems, which must be solved by the students and implemented in the laboratory. The practice groups will have a maximum of 16 students which will work in pairs. During the practice session, the two students of every spot must participate actively in the assembly (and/or the simulation) of the circuits. At the end of every session, the lecture will take down notes with the right realization of the corresponding practice.

6. Detailed Contents:

Didactical unit I: Introduction basic concepts

Chapter 1: Introduction to the digital systems.
1.1 Definition of system.
1.2 Analogic and digital systems.
1.2.1 Positive and negative logic.
1.3 Types of digital systems.
1.4 Positional numbering systems.
1.4.1 Decimal, binary, octal and hexadecimal systems.
1.4.2 Conversion between the different numbering bases.
1.5 Encoding.
1.5.1 BCD codes.
1.5.2 Continuous or progressive codes.
1.5.3 Cyclic codes.
1.5.4 Error-detecting codes.
1.5.5 Error-correcting codes.

Chapter 2: Boole algebra, binary logic and logic gates.
2.1 Definition and postulates of Boole algebra.
2.2 Fundamental theorems of Boole algebra.
2.3 Logic functions.
2.3.1 Truth table of a logic function.
2.3.2 Canonical forms of a logic function.
2.3.3 Conversion between the canonical forms of a logic function.
2.3.4 Logic incomplete functions.
2.4 Logic gates.
2.5 Realization of logic functions via logic gates.
2.6 High impedance outputs.

Didactical unit II: Combinational and arithmetic systems

Chapter 3: Analysis and design of combinational circuits.
3.1 Introduction to the combinational systems.
3.2 Stationary analysis of combinational circuits with logic gates.
3.3 Design of combinational circuits with logic gates.
3.3.1 Minimization of completely-specified functions.
3.3.2 Minimization of incomplete functions.

Chapter 4: Combinational functional blocks.
4.1 Introduction to the combinational functional blocks.
4.2 Decoders
4.2.1 Decoder expansions.
4.2.2 Realization of logic functions with decoders.
4.2.3 BCD to 7-segment converters.
4.3. Encoders.
4.3.1 Encoder expansions.
4.4. Multiplexers.
4.4.1 Multiplexer expansions.
4.4.2 Realization of logic functions with multiplexers.
4.5. Demultiplexers.
4.6 Comparators.

4.6.1 Comparator expansion.
4.7 Parity generators/checkers.
4.7.1 Parity generators/checkers expansion.
4.8 Design-based in combinational functional blocks.

Chapter 5: Binary arithmetic.
5.1 Representation of signed-numbers.
5.1.1 Sign-magnitude.
5.1.2 One's complement.
5.1.3 Two's complement.
5.2 Binary sum.
5.2.1 Adder circuits.
5.2.2. Adders expansion.
5.3 Binary subtract.
5.3.1 Subtractor circuit in two's complement.
5.3.2 Adder/subtractor circuit.
5.4 Arithmetic-logic units (ALUs).

Didactical unit III: Sequential systems
Chapter 6: Introduction to the sequential systems.
6.1 Definition of sequential system.
6.2 Representation of the sequential systems.
6.2.1 State diagrams.
6.2.2 State tables.
6.3 Classification of the sequential systems.
6.3.1 Synchronous and asynchronous digital systems.
6.3.2 Mealy and Moore machines.
6.4 Bistable circuit.
6.4.1 Asynchronous bistable circuit.
6.4.2 Latches.
6.4.3 Flip-flops.
6.4.4 Timing constraints of the bistable circuits.

Chapter 7: Systems' analysis and design with bistable circuits.
7.1 Analysis of systems with bistable circuits.
7.2 Design of systems with bistable circuits.
7.2.1 State encoding in natural binary.
7.2.2 State encoding in 1-out-of-n.

Chapter 8: Sequential functional blocks.
8.1 Registers.
8.1.1 Registers with load enable and with parallel load.
8.1.2 Shift registers.
8.1.3 Sequential design based on registers.
8.2 Counters.
8.2.1 Synchronous counters.
8.2.2 Asynchronous counters.
8.2.3 Counters expansion.

Didactical unit IV: Programmable logic
Chapter 9: Programmable structure and memories.
9.1 Introduction to the programmable logic.
9.2 PLA structures.

9.3 PAL structures.
9.4 PROM memories.
9.5 RAM memories.
9.5.1 Static RAM memories (SRAM).
9.5.2 Dynamic RAM memories (DRAM).
9.6 NVRAM memories.
Laboratory practices
Practice 0: Contact with the laboratory material.
Practice 1: Realization of logic functions with SSI devices (I).
Practice 2: Realization of logic functions with SSI devices (II).
Practice 3: Realization of logic functions with MSI devices (I).
Practice 4: Realization of logic functions with MSI devices (II).
Practice 5: Design of combinational systems with hardware description languages.
Practice 6: Design of sequential systems with hardware description languages (I).
Practice 7: Design of sequential systems with hardware description languages (II).

7. Bibliography

7.1. Basic Bibliography

- Fundamentos de Sistemas Digitales. T. L. Floyd, Ed. Prentice-Hall.
- Sistemas Digitales y Tecnología de Computadores. J.M. Angulo, J. García Zubía. Ed. Thomson.
- Sistemas Electrónicos Digitales. E. Mandado. Ed. Marcombo.
- Diseño Digital, Principios y Prácticas. John F. Wakerly. Ed. Prentice Hall. Fundamentos de Diseño Lógico. C.H. Roth. Ed. Thomson.
- Fundamentos de Diseño Lógico y Computadores. M. Morris Mano, Charles R. Kime. Ed. Prentice Hall.

7.2. Additional Bibliography:

- Problemas Resueltos de Electrónica Digital. J. García Zubía. Ed. Thomson.
- Problemas de Circuitos y Sistemas Digitales. C. Baena y otros. Ed. McGraw Hill.

8. Systems and Assessment Criteria

8.1. System for Assessment:

- Problems / theory exam
- Practice presentation
- Practice exam

8.2. Assessment Criteria and Marks:

Theoretical part assessment:
The theoretical part mark will contribute in a 65% to the course final mark and will be carried out by means of two tests: a test-type exam and a problem exam. These test will take place in the ordinary course session calls I (February), II (currently September) and III (December). The student can make use of two session call at maximum in every academic year. Once any part has been passed the achieved marks will be keep till the session call II (September) of every academic year. Test-type exam: this test will consist of a set of questions concerning the theoretical concepts lectured in the course. The wrong answers may subtract points in the

exam mark. The weight of the test-type exam in the final mark will be a 20%. (Competences which are assessed: CB03, CC09, CG0 and CT2). Problem exam: In this test, the student must apply the different methodologies of analysis and/or design to solve some representative problems of the program lectured in the course. The weight of the problem exam in the final course mark will be a 45%. (Competences which are assessed: CB03, CC09, CG0, G03 and CT2).

Laboratory practices mark: The Laboratory practices mark will contribute with a 35% to the course final mark and in the continuous assessment modality it will be conducted by means of the mixture of the two assessment systems which follow:

Practices' defense: The attendance to the laboratory sessions will be mandatory to the course practical part. Every group will be composed of two partners who must introduce the lecturer the circuits' right operation belonging to the different practices. To pass the laboratory practices, the student must do rightly at least 5 out of the 7 proposed practices in this part. The weight of the practice defense in the course final mark will be 24.5%. (Competences which are assessed: CB03, CC09, CG0, G03, G04, G05, G06, G08, CT2, CT3 and CT4).

Practices' exam: Those students who, having done rightly at least 5 practices in the practices' defense, would like to get a higher mark, must attend to a practices' exam (from the part corresponding to the design with VHDL) which will be held in the first exam session call (February). The practices' exam weight in the course final mark will be 10.5%. (Competences which are assessed: CB03, CC09, CG0, G03, G04, G08, CT2 and CT4).

The laboratory practices' final mark will be computed by means of the sum of the achieved marks in the practices' defense and the practices' exam. The laboratory practices, once passed, its mark will be saved till the third exam session call (December) of the upcoming academic year. Those students who do not pass the laboratory practices in the February session call following the previous procedure can attend to a global practices' exam, which will take place in the second session call (nowadays September) of the third session call (December) for those students who rejoin the course, and which will be composed of two parts: assembly and VHDL design. In this exam, the student must pass both parts to pass the practices. On the whole, and once the theoretical part and the laboratory practices are passed, the course final mark will be computed with the following mathematical relationship: Final mark: 0.20 x Type-test exam + 0.45 x Problem exam + 0.245 x Practices' defense + 0.105 x Practices' exam

Single final assessment: Those students who during the two first weeks of the course lecturing (or during the two following weeks to his/her enrollment, if it had been take later than the course starting) inform suitably the lecturer (written or via the corporative email from the University of Huelva) will have right to take part in a single final assessment, renouncing in an irreversible way to the continuous assessment system followed during the four-month period. This single final assessment test will be conducted in the ordinary exam session calls: I (February), II (currently September) and III (December) of the course; every student is allowed to make use of two session calls, at maximum, in every academic year.

The test will contain a test-type exam and a problem exam (its marks, once passed, will be saved till the second exam session call (September) and will contribute to the final mark with weights of a 20% and a 45%, respectively) and a laboratory practices' exam (its mark, once passed, will be saved till the third exam session call (December) of the upcoming academic year and will contribute to the course final mark with a weight of a 35%).The test-type exam will consist of a set of questions concerning the theoretical concepts lectured in the course. In the problem exam, the student must apply the different methodologies of analysis and/or design to solve some representative problems of the program lectured in the course. The practices' exam will have two parts. In the first part the student must do the design of a digital

system and its right implementation in the practices' trainer. In the second part, the student must conduct the digital system modeling in VHDL language and to check its right operation by simulating it.

Honors: Concerning the honors' granting, for every session call of the academic year, it can only be done whether in the previous session calls of the same academic year had not been yet assigned the maximum possible number of honors (which will depend on the enrolled students' number). Furthermore, if in a certain session call there would be more candidates to honors than granting possibilities, the honors will be granted to those students with the greatest final marks, and in equity case, to those students who have reached a higher mark in the theoretical part.